

SLE Interlaken IP Key Features:

- Conforms to Interlaken Protocol Definition, Rev. 1.2
- Meets Interlaken Alliance Interop Recommendations, Rev. 1.3
- Supports 256 logical channels, plus 8-bit channel extension for up to 64K channels
- SerDes lanes may be individually enabled/disabled
- Supports the full range of Interlaken SerDes speeds (3.125Gbps to 10.3125Gbps)
- Three options for User Interface (128 bit, 256 bit, and 2x256 bit) allow for high bandwidth at lower core clock speed
- BURSTMAX size can be configured from 64 bytes up to 512 bytes
- BURSTMIN size can be configured from 32 bytes up to 256 bytes
- Supports both in-band and out-of-band flow control
- Internal and external loop-back paths on both data and flow control
- Error detection on user interface to detect illegal burst sizes and other errors
- Configurable error injection mechanisms for testability
- Supports both packet mode and segment mode
- Generic SerDes interface can attach to SerDes for many different vendors
- Parameterized SerDes width can support 8, 10, 16, 20, or 32 bits

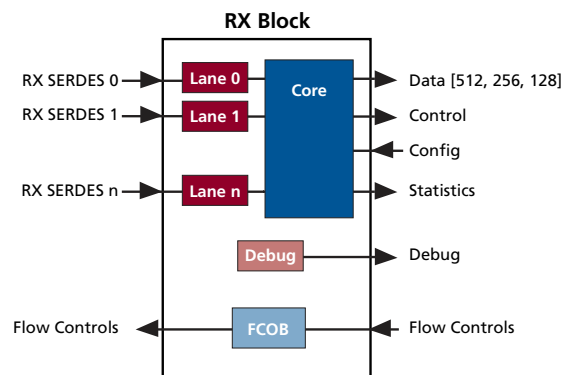
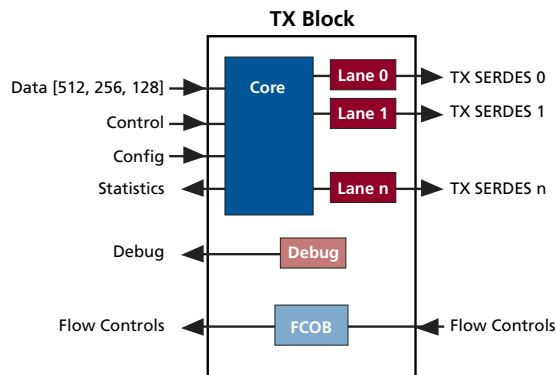
SLE Interlaken

Interlaken is a scalable, high-speed chip-to-chip interface protocol that combines the advantages of popular SPI-4.2 and XAUI interfaces. It builds on the channelization and per channel flow control features of SPI4.2, while reducing the number of chip I/O pins by using high-speed SerDes technology, similar to XAUI.

SLE's scalable Interlaken IP Core provides from 10Gbps to over 150Gbps of bandwidth. This scalability ideally suits Interlaken for multiple generations of future network switches, routers and storage equipment. The scalability is achieved through the combination of SerDes speed (3.125Gbps to 10.3125Gbps) and a variable number of SerDes lanes (1 to 24).

Designed and tested to be easily synthesizable into many ASIC technologies, SLE's Interlaken IP Core was uniquely built to work with off-the-shelf SerDes from most leading technology vendors. Using the vendor specific, proven, SerDes allows SLE customers to quickly integrate the Interlaken IP Core into the customer's technology of choice.

Interlaken Top Level Block Diagram



SLE Interlaken IP

Key Features

(continued):

- Built-in interrupt structures
- Maintenance interface for control and configuration, interrupts and status, SerDes debug, programmable calendar and flow control, and statistics counters

Ordering Information:

For pricing and availability information, please contact SLE at sales@siliconlogic.com.

More Information

The open Interlaken specification was co-written by Cortina Systems and Cisco Systems to provide a far more scalable chip-to-chip interface protocol than previous protocols. Interlaken combines the advantages of the popular SPI4.2 and XAUI interfaces by building on the channelization and per-channel flow control features of the SPI4.2, and reducing the number of chip I/O pins by using high-speed SerDes technology, similar to XAUI.

For more information regarding the Interlaken technology download: Interlaken Technology: New Generation Packet Interconnect Protocol — White Paper www.siliconlogic.com/pdfs/Interlaken_White_Paper-March_2007.pdf

The SLE licensable Interlaken IP is available through SLE's sales network.

For sales related questions, contact sales@siliconlogic.com or call 1-908-580-1870.

About SLE

Silicon Logic Engineering, Inc. (SLE) specializes in right-first-time design services that address all aspects of ASIC, FPGA and semiconductor system design services. SLE's proven and repeatable Think Physical™ design process, tools and semiconductor intellectual property reduce time-to-market and are provided by one of the most experienced VLSI design services teams in the industry. SLE is a division of Tundra Semiconductor Corporation (TSX:TUN). For more information about SLE, please visit www.siliconlogic.com.



Silicon Logic Engineering, Inc.
7 South Dewey Street
Eau Claire, Wisconsin 54701

Phone: 715-830-1200
Fax: 715-830-1887
Email: sales@siliconlogic.com

www.siliconlogic.com

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