Silicon Logic Engineering
A Division of Tundra Semiconductor

# SPI-4 Phase 2:

## POS-PHY Level 4

### Features:

- Conforms to Optical Internetworking Forum Specification System Packet Interface Level 4 Phase 2 standard (OIFSPI4-02.0)
- Implementation is technology independent; currently available in several technologies, portable to others
- Fully testable synchronous design operates up to 1000 Mb/s per line
- Supports dynamic bit de-skew over full frequency range
- Incorporates a fully digital design which is implemented in standard cell ASIC libraries using no custom cells, no analog components, no PLLS, and no DLLs
- Incorporates a proprietary real-time tuning feature which reduces the need for periodic training, increases usable bandwidth, and improves data integrity
- Features a high-speed digital SerDes for technology portability and faster time-to-market
- Manages up to 256 ports and supports calendar lengths up to 1024, allowing for uneven bandwidth allocation across channels
- Performs credit management and arbitration to ease user logic design and accelerate time-to-market
- Incorporates an asynchronous interface between the user clock and the SPI-4.2 channel clock to ease user logic design and accelerate time-to-market
- Allows for per-port configurable maxburst values creating maximum flexibility in bandwidth allocation

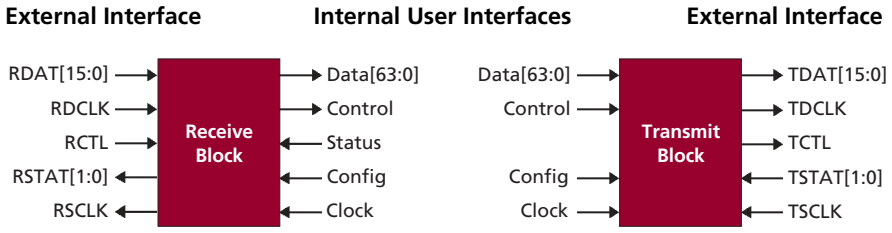
### SLE SPI-4 Phase 2

The SPI-4 Phase 2 (System Packet Interface Level 4 Phase 2) is a high-speed interconnection for 10+ Gb/s aggregate bandwidth applications. It provides for packet and cell transfer in applications such as OC-192 ATM, Packet over Sonet/SDH, as well as 10 Gb/s Ethernet.

Silicon Logic Engineering's SPI-4.2 receiver and transmitter blocks provide a complete solution for the customers' applications, from physical layer bit de-skew through the link-layer protocol management. This includes all OIF-required features for the full solution and some additional features for easier implementation and integration.

These full-featured designs provide the functionality and flexibility required to speed time-to-market.

### SPI-4 Phase 2 Top Level Block Diagram




### Functional Description

#### The Receive Block (RX)

The RX block manages all tasks associated with the receiving of data from the SPI-4.2 interface. Some of these tasks include:

- Managing and interpreting the command protocol, receiving 16 bit data words, and combining them into 64 bit aligned words for transfer to the user
- Parsing control words and providing sideband indications to the user for SOP, EOP status, and bad parity
- Calculating and checking the incoming DIP-4 error protection codes and managing synchronization by requesting training from the transmitter when a programmable threshold of DIP-4 errors has been reached
- Receiving and storing port status information from the user
- Sending the status information on the outgoing status channel according to programmable calendar, generating and inserting DIP-2 parity and framing as appropriate
- Recognizing the incoming training pattern on the data interface and performing bit de-skew when needed

## Features (continued):

- Simple flow-through user architecture allows for design and implementation flexibility and highly configurable operation
- Optimized for high-speed ASICs
- Deliverables include packet generator and protocol checker

## Deliverables:

- Synthesizeable Verilog RTL for link layer
- Gate-level design for physical layer
- Sample synthesis scripts
- Behavioral models
- Timing constraints
- Documentation
- Available for most verilog simulators
- SPI-4.2 Packet Generator
- SPI-4.2 Protocol Checker

## Ordering Information:

For pricing and availability information, please contact SLE at sales@siliconlogic.com.

## Functional Description (continued)

### The Transmit Block (TX)

The TX block manages all tasks associated with the sending of data on the SPI-4.2 interface. Some of these tasks include:

- Accepting 64 bit data words from the user to transmit them on the SPI-4.2 interface
- Generating and inserting appropriate SPI-4.2 control words, based on sideband information from the user, indicating SOP, EOP, and bad parity
- Calculating and sending the outgoing DIP-4 error protection codes
- Receiving and managing status channel information
- Performing credit management using per port configurable maxburst values and the status received, decrementing credit counters as data is sent
- Performing arbitration for up to 256 ports using a round-robin algorithm that gives priority to starving ports, using the status received and a vector from the user indicating which ports have data to send
- Generating periodic training according to a user-programmable data_max_t configuration parameter
- Providing a buffer of configurable depth on the internal user interface to minimize or eliminate stalls in transferring data to the SPI-4.2 block
- Maintaining synchronization with the SPI-4.2 receiver by sending training on the data interface in response to framing pattern on the status interface or when a programmable threshold of DIP-2 parity errors is exceeded on the status interface

## About SLE

Silicon Logic Engineering, Inc. (SLE) specializes in right-first-time design services that address all aspects of ASIC, FPGA and semiconductor system design services. SLE's proven and repeatable Think Physical™ design process, tools and semiconductor intellectual property reduce time-to-market and are provided by one of the most experienced VLSI design services teams in the industry. SLE is a division of Tundra Semiconductor Corporation (TSX:TUN). For more information about SLE, please visit www.siliconlogic.com.

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