

The logo for ASICBlaster™ toolsuite. "ASICBlaster™" is in a white, sans-serif font, and "toolsuite" is in a smaller, grey, lowercase, sans-serif font below it. The background is a dark blue gradient with a faint white circuit board pattern.

# ASICBlaster™ toolsuite

ASICBlaster toolsuite is a suite of point tools developed in house to bridge gaps and increase productivity, enabling SLE to be more efficient and to achieve better results on leading-edge designs. Each tool addresses a specific problem within the ASIC design process. The tools are optimized to work on large, high-speed ASIC designs.

They are designed to work with, not compete against, existing industry-standard ECAD tools.

## Featuring DelayBlaster™

DelayBlaster is a timing optimization tool that takes over where other tools leave off. It is designed for use late in the ASIC design cycle to clean up paths missing by multiple nanoseconds, or after a route to close on those last few picoseconds of negative slack. DelayBlaster minimizes disruption to the design by only making changes absolutely required, and by allowing the user to choose the types of changes that can be tolerated at a given point in the design cycle.

DelayBlaster works in unison with other industry-standard tools. It relies on input from a static timing tool and produces scripts to be used with existing synthesis and placement tools to implement changes. The changes include resizing of existing gates and insertion of buffers and inverters (logically and physically) to speed-up the long paths.

## Benefits

- Integration with industry-standard tools via simple text-based files
- Exact correlation with the static timing tool, since DelayBlaster uses timing data from the static timing tool directly
- Simple yet effective algorithms mean fast run-times with excellent QoR
- Flexible input parameter file allows user to easily control which violations are looked at, as well as the types of fixes that can be implemented
- Proven for use with large, complex ASICs (10M+ gates, 400+ MHz)
- Preservation of logic with a "dont\_touch" attribute
- Ability to process hierarchical or flat designs
- Correction of technology violations, either implicitly or explicitly, during an optimization run



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