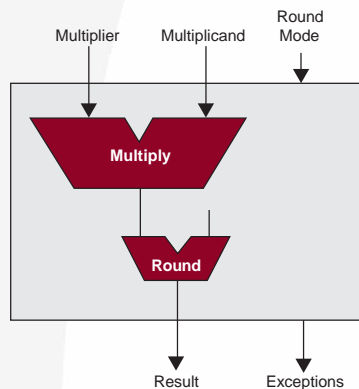


# Floating Point multiply unit



## Features

- IEEE-like Arithmetic (Denormals treated as Zeros)
- IEEE Single Precision Format
- Fully Combinational Design

## Description

The Floating Point Multiply Unit is optimized to exclusively support the multiplication operation.

The operation of this unit follows the IEEE 754 Standard for Floating Point Arithmetic for Single Precision (32-bit) arithmetic with the exception that Denormals are treated as like-signed Zeros. An additional exception flag is provided to signal when a Denormal input or what would have been a Denormal output is flushed to Zero. Results for exceptions are the IEEE Standard default results as defined for the case when no trap occurs.

The Floating Point Multiply Unit is a fully combinational unit. The design is coded in a pipelined fashion, and pipeline registers may be easily added to support high clock frequencies.

NaN formats may be specified with a configurable QNaN bit value and bit position, and a default QNaN may be specified for Invalid results.

The signaling of Underflow is configurable for the detection of tininess either before or after rounding.

The Floating Point Multiply Unit is designed to provide the Multiply operation with minimal latency, at the expense of some extra area.

The approximate gate count and latency for the Floating Point Multiply Unit is 7,400 gates and 5.0 ns for a typical 0.18 micron Standard Cell technology.

## Applications

- Microcontrollers
- Microprocessors



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